H

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,268	10/22/2001	Jeng-Jye Shau	SHAU-0103	8393

7590 08/13/2004

EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	

Bo-In Lin
13445 Mandoli Drive
Los Altos Hills, CA 94022

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,268	SHAU, JENG-JYE	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-16* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1 and 2, drawn to A method for changing a configuring of an error correction code (ECC) logic circuit comprising sequentially interconnecting a set of N1 identical error-check blocks and figuring said ECC logic circuit by changing said ECC logic circuit to a set of N2 sequentially interconnected circuits, classified in class 714, subclass 774.

II. Claims 3 and 4, drawn to A method for operating a memory device comprising repairing a faulty memory cell storing an error data bit, classified in class 714, subclass 710.

III. Claims 5-10, drawn to A memory device comprising an error-check logic circuit includes a set of identical error-check blocks sequentially interconnected for checking errors of data storage in said memory cells, classified in class 714, subclass 757.

IV. Claims 11-14, drawn to A content addressable memory (CAM) device comprising an error-check logic circuit for checking errors of said data access to each of said memory-cell arrays, classified in class 714, subclass 763.

V. Claim 15, drawn to A memory device comprising a multiple-level electrical-charge sensing means for sensing at least two electric-charge levels stored in said floating gates, classified in class 365, subclass 201.

VI. Claim 16, drawn to An analog sensing device comprising an analog signal sensing means for sensing a sequence of analog signal-levels for generating a sequence of bit patterns, classified in class 714, subclass 738.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I, II, III, IV, V and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as amethod for changing a configuring of an error correction code (ECC) logic circuit comprising sequentially interconnecting a set of N1 identical error-check blocks and figuring said ECC logic circuit by changing said ECC logic circuit to a set of N2 sequentially interconnected circuits. In the instant case, invention Group II has separate utility such as repairing a faulty memory cell storing an error data bit. In the instant case, invention Group III has separate utility such as a memory device comprising an error-check logic circuit includes a set of identical error-check blocks sequentially interconnected for checking errors of data storage in said memory cells. In the instant case, invention Group IV has separate utility such as a content addressable memory (CAM) device comprising an error-check logic circuit for checking errors of said data access to each of said memory-cell arrays. In the instant case, invention Group V

has separate utility such as a memory device comprising a multiple-level electrical-charge sensing means for sensing at least two electric-charge levels stored in said floating gates. In the instant case, invention Group V has separate utility such as an analog sensing device comprising an analog signal sensing means for sensing a sequence of analog signal-levels for generating a sequence of bit patterns. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I, II, III, IV, V and VI is mutually exclusive, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

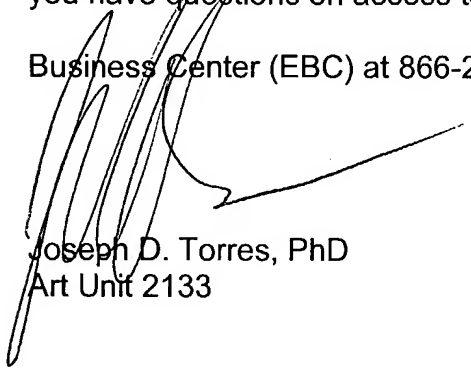
A telephone call was made to Bo-in Lin on 26 July 2004 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Art Unit 2133